

## **Wafer Edge Defect Inspection**

### Field of the Invention

This invention relates to wafer defect inspection within fabrication systems that form integrated circuits (ICs) on semiconductor wafers. In particular, this invention relates to new and improved techniques for inspecting the edges of the wafers for defects preferably between various process steps during the over-all fabrication of the wafers within the fabrication system.

### Background of the Invention

A significant trend throughout IC development has been to try to increase the "yield rate" of semiconductor fabrication systems. The yield rate refers to the percentage of usable IC's produced by a fabrication system compared to the total number attempted. Similarly, the yield rate may refer to the percentage of usable IC's obtained from an average semiconductor wafer that is processed through the fabrication system. A semiconductor wafer is essentially a thin disc of highly purified semiconductor material on which many IC's are fabricated together and then separated for individual packaging.

Significant factors that can negatively impact the yield rate are the number and size of defects in the wafer. Defects may include cracks, crazes (i.e. microscopic cracks), chips, flakes, scratches, marks, missing/broken edges and particle and residue contamination, among others. Defects are particularly detrimental to the yield rate when they occur on the top surface of the wafer, since the top surface is the region where the IC's are formed on the wafer. Of historically lesser concern have been any other areas of the wafer, such as the bottom surface and the edge, or bevel, of the wafer. Since these areas are further from the formation of the IC's, any defects therein have been considered to have less of an impact on the yield rate for the IC's. Thus, many wafer-inspection and defect-

detection techniques have been developed to inspect for defects in the top surface of wafers; whereas, comparatively few techniques have been developed to inspect for defects elsewhere on the wafers.

Until recently, wafer edge inspection has primarily been performed by manual visual inspection by a worker in the fabrication plant. A high-resolution camera may be used to generate an image of the wafer edge on a monitor, which the worker manually views for defects. This edge inspection technique is in stark contrast to the various complex computerized image-analysis techniques, among other inspection techniques, that have been developed to inspect the top surface of the wafers. Recent developments in non-visual inspection of wafer edges have merely included emitter/detector pairs for ultrasonic waves and laser/light beams for limited detection of cracks and breaks at the edge. These techniques may be used in combination with visual inspection to confirm the presence of any defects in the wafer edge. Detailed image-analysis techniques have not been used for wafer edge defect detection, since it has been commonly considered unnecessary to do so.

Additionally, current non-visual wafer edge inspection techniques may record data plots (not images), which a worker may review for indications of defects or a computer may analyze for possible defects. Though the data may be stored for a time, the purpose of the data is generally for immediate pass/fail analysis of the wafer, so the wafer may be passed on for further processing, discarded as unusable or rerouted for rework or repair.

It is with respect to these and other considerations that the present invention has evolved.

#### Summary of the Invention

The present invention arose out of the recognition of the importance of wafer edge defects relative to yield rate and the need to give greater consideration to edge defects during wafer fabrication. It was realized that defects at the edge of a wafer, though they are far from the IC's on the surface of the wafer, frequently cause problems in the fabrication of the IC's. For instance, process-induced edge

contamination and flaking from the wafer edge are types of defects that can cause considerable problems in IC fabrication, particularly when particles or flakes break off of the edge and land on the top surface of the wafer during a process step.

5 Additionally, cracks in the wafer edge may propagate to the interior of the wafer, particularly during process steps that thermally cycle the wafer. Furthermore, with the introduction of new wafer processing technologies such as the use of low-K dielectrics and copper dual damascene processes, new and more pronounced edge related defect mechanisms, or causes, (e.g. film separation during thermal processing, stress induced de-lamination, changes to film properties during  
10 subsequent process steps, etc.) have occurred. Therefore, there is a need for wafer edge inspection that goes beyond the limited capabilities of the visual inspection techniques and emitter/detector pair techniques described above.

Visual inspection of the edges has proven to be too time-consuming and unreliable to adequately address the problem of wafer edge defects during the  
15 over-all fabrication process. Additionally, the emitter/detector pair techniques detect too limited of a range of types of defects. For instance, the process-induced edge contamination and the flaking from the wafer edge are types of defects that the emitter/detector pair techniques cannot detect.

Furthermore, it was realized that a system of storing and managing  
20 inspection data for future analysis is necessary to perform a detailed investigation of the efficiency of the over-all fabrication system in order to optimize each process step within the fabrication system and maximize the yield rate. The inspection techniques heretofore developed do not include such a feature.

According to various embodiments, therefore, the present invention  
25 preferably involves methods and apparatus for automatic image-capture, image-data-storage and image-analysis using a database within which the image data is stored and managed. The image data is preferably accessible for comparison and analysis of wafers at different points in the fabrication system so that the effects of a given process step on the addition or repair of edge defects can be determined.

30 Additionally, the image data is preferably accessible for comparison and analysis of

different wafers at the same point in the fabrication system so that the effects of changing a given process step can be determined.

According to certain embodiments, the present invention preferably includes an image capturing device, such as a scanning electron microscope or an optical review system (e.g. a camera, etc.). The image capturing device sends wafer edge images to the database. Preferably more than one image capturing device (or an inspection station within which the image capturing device is incorporated) is located within the fabrication system relative to selected fabrication stations within which particular process steps are performed. Using a workstation, or computer, a user preferably accesses the wafer edge images and instructs the computer to perform a variety of analyses on one or more images at a time to discover the effects of various process steps in the fabrication system.

A more complete appreciation of the present invention and its scope, and the manner in which it achieves the above noted improvements, can be obtained by reference to the following detailed description of presently preferred embodiments of the invention taken in connection with the accompanying drawings, which are briefly summarized below, and the appended claims.

#### Brief Description of the Drawings

Fig. 1 is a simplified schematic of a fabrication system having inspection stations and in which the present invention is incorporated.

Fig. 2 is a simplified schematic of an enlargement of a portion of the fabrication system, including the inspection stations, shown in Fig. 1.

Figs. 3, 4 and 5 are simplified plan views of alternative embodiments for the inspection stations shown in Figs. 1 and 2.

Fig. 6 is a simplified plan view of a semiconductor wafer to be processed by the fabrication system shown in Fig. 1 and inspected by one or more of the inspection stations shown in Figs. 1-5.

Fig. 7 is a simplified elevation view of the wafer shown in Fig. 6 and an image capturing device incorporated in the inspection stations shown in Figs. 1-5.

Fig. 8 is exemplary inspection result graphs of defects on an edge of the wafer shown in Figs. 6 and 7

### Detailed Description

An exemplary fabrication system 100 that fabricates integrated circuits (IC's) (not shown) on semiconductor wafers (not shown) is shown in Fig. 1. The fabrication system 100 includes several conventional fabrication machines, or stations, 102-114, such as metal deposition devices, ion implantation devices, epitaxial growth chambers, ovens, spin-on-glass devices, etc. Thus, the fabrication stations 102-114 perform various conventional process steps in a specific processing order on the wafers in order to fabricate the IC's. The fabrication system 100 also includes inspection systems 116-122. Each inspection system 116-122 is interposed between two fabrication stations 102-114 to intercept one or more or all of the wafers passing between the fabrication stations 102-114 for inspection purposes. Each inspection system 116, 118, 120 and 122 corresponds to the fabrication station 104, 106, 112 and 114, respectively, that immediately precedes it in the processing order. The inspection systems 116-122, thus, inspect the wafers within the fabrication system 100 after specific processing steps have been performed in the corresponding fabrication stations 104, 106, 112 and 114. The inspection systems 116-122 inspect and analyze the wafers for defects in the edges thereof at selected points in the fabrication system 100 using image-capture and image-analysis. The inspection systems 116-122 may also categorize the type of each wafer edge defect detected through the inspection and analysis. Exemplary types of wafer edge defects that can be detected by the inspection systems 116-122 include cracks, crazes (i.e. microscopic cracks), chips, flakes, scratches, marks, missing/broken edges and particle and residue contamination, among others.

The inspection systems 116-122 are preferably located within the fabrication system 100 to enable a user or operator of the fabrication system 100 to evaluate the performance of the fabrication system 100 at selected points therein with respect to wafer edge defects. The information obtained further enables the user

to evaluate the performance of individual fabrication stations (e.g. 106) by having inspection systems (e.g. 116 and 118) immediately upstream and downstream of the fabrication station 106, so that “before” and “after” wafer edge defect data can be compared together to determine whether the process step performed by the fabrication station 106 detrimentally adds new defects to the wafer edge or beneficially repairs preexisting defects. Similarly, the information obtained enables the user to evaluate the performance of groups of fabrication stations (e.g. 108, 110 and 112) by placing inspection systems (e.g. 118 and 120) immediately upstream and downstream of the group of fabrication stations 108, 110 and 112. Such “before” and “after” wafer edge defect data is generally obtained by inspecting the same wafer, or set of wafers, both before and after the selected fabrication station 106 or group of fabrication stations 108-112 and comparing both inspection results.

The information obtained by the inspection systems 116-122 also enables the user to evaluate the effect of making adjustments to one or more of the fabrication stations 102-114. The adjustment-effect evaluation is generally done by inspecting different wafers processed by the same fabrication station 104, 106, 112 or 114 by the inspection station 116, 118, 120 or 122 corresponding thereto both before and after the adjustment is made and comparing average results.

With the information obtained and the evaluations and analyses thereof, the user can adjust the performance of some or all of the fabrication stations 102-114 to increase the efficiency, throughput and yield rate of the over-all fabrication system 100. For instance, the wafer edge defect analyses may reveal to the user that particular adjustments to one or more of the fabrication stations 102-114 can reduce the number or severity of defects added either by the adjusted fabrication station(s) 102-114 or even by another non-adjusted fabrication station 102-114. Additionally, some adjustments to some of the fabrication stations 102-114 may prove to repair some wafer edge defects. Therefore, if it is too costly to adjust one fabrication station 102-114 to reduce added defects, it may be possible to adjust a different fabrication station 102-114 to compensate for the added defects.

Additionally, the wafer edge defect analyses may indicate to the user that certain process steps within one or more of the fabrication stations 102-114 result in certain types of reparable defects, so the user can add one or more fabrication stations to clean, rework or repair the wafers after these process steps. For instance, edge contamination, such as may be caused by contact with a Teflon, or like polymer, edge material of the wafer cassette (e.g. reference 146, Fig. 3, see below) or by another process that contacts or impacts the wafer edge, may be reparable by removing the wafer from the regular process flow and passing the wafer through an edge cleaning or polishing process. After such remedial measures, the wafer may be returned to the regular process flow.

The fabrication system 100 could potentially have enough inspection stations 116-122 to obtain a before-and-after analysis of each process step, or fabrication station 102-114. However, due to space, time and money constraints, it is unlikely that such a case could be achieved for most fabrication systems. Therefore, the selections for the placements of the inspection systems 116-122 depends on which process steps, or fabrication stations 102-114, the user, or designer of the fabrication system 100, considers to be most critical. Additionally, it may be possible for a single inspection system (e.g. 118) to inspect wafers at more than one point in the fabrication system 100, as indicated by the dashed line connected to inspection system 118, thereby allowing the inspection system 118 to perform double-duty. After the most critical process steps, or fabrication stations 102-114, have been analyzed and perhaps adjusted, the inspection systems 116-122 may be moved to other locations in the fabrication system 100 for additional inspection.

The inspection systems 116-122 may remain at the most critical locations within the fabrication system to continue to monitor the performance of some of the fabrication stations 102-114. However, when the fabrication system 100 has proven to be relatively optimized for performance and yield rate, it may be possible to remove some or all of the inspection systems 116-122 from the fabrication system 100 to reduce cost, time and complexity of the over-all fabrication. On the

other hand, when the fabrication system 100 exhibits deterioration in its performance, it may be necessary to add inspection systems 116-122 to the fabrication system 100 to diagnose the cause of the deteriorating performance.

The inspection systems 116-122 preferably involve an inspection station 124, a database 126 and a workstation 128, as shown for the exemplary inspection system 116 in Fig. 2. The inspection station 124 is interposed between the preceding fabrication station 104 and the subsequent fabrication station 106 to receive some or all of the wafers (not shown) passing in the process order from the preceding fabrication station 104 to the subsequent fabrication station 106. The database 126 and the workstation 128 may preferably be shared by all of the inspection systems 116-122 (Fig. 1). Additionally, the database 126 and the workstation 128 may be physically located away from the inspection stations 124 and the fabrication stations 102-116, since the database 126 and the workstation 128 do not have to be within a clean-room environment as required for the parts of the fabrication system 100 (Fig. 1) that handle the wafers. The workstation 128 is preferably a conventional general-purpose computer. The database 126 is preferably a conventional computerized mass-storage system.

The inspection station 124 receives the wafers (not shown) and generates "raw" inspection data, preferably digital images, of the wafers. The inspection data is transferred to the database 126 for storage and management. For ease of searching, the stored inspection data for each inspected wafer is correlated with and searchable by an identification (ID) for the wafer and an ID for either the inspection station 124 that took the data, the fabrication station (e.g. 104) preceding the inspection station 124 or the process step performed by the preceding fabrication station 104. The ID for the wafer may include an ID for a "wafer lot" from which the wafer originated and the wafer's ID within the wafer lot.

Using the workstation 128, a user accesses the stored data for one or more wafers and one or more process steps and instructs the workstation 128 to perform various edge defect analyses. For example, the analyses determine whether any defects exist in the edge of one or more of the wafers, whether any defects have



been added to the edge of a wafer between two inspection stations 124, whether any defects have been repaired (i.e. “negative adders”) on the edge of the wafer by the process step(s) between two inspection stations 124, whether a process step is still causing wafer edge defects even after the process step has been adjusted, etc.

5           To perform these types of analyses, it is necessary to maintain the inspection data within the database 126 for every wafer for a proper amount of time. In fact, the user may not instruct the workstation 128 to perform these analyses until several minutes or hours after the data has been generated. Therefore, storage of the inspection data is more important for the present  
10           invention than it was for the prior art wafer edge defect detection techniques described in the background, which were only concerned with immediate edge defect detection after a given process step, so the inspection data could be immediately deleted thereafter. Thus, the database 126 enables more thorough defect inspection of each wafer and more thorough analysis of the over-all  
15           performance of the fabrication system 100 (Fig. 1).

          The analyses of the inspection data may involve conventional image-analysis techniques, such as comparing a recorded image to an ideal image to determine any differences, which may indicate various types of anomalies in the recorded image. Thus, the recorded image of the edge of a selected wafer is  
20           preferably compared to an image of an ideal wafer edge to generate defect data indicating the locations of possible defects on the edge of the selected wafer.

          For a wafer that has been inspected both before and after one or more process steps, “before” and “after” edge defect data can be generated for the wafer and compared together to determine the effect of the intervening process step(s).  
25           For example, defect data that indicates more and/or larger defects in the “after” data indicates that the intervening process step(s) added defects to the edge of the wafer. On the other hand, defect data that indicates fewer and/or smaller defects in the “after” data indicates that the intervening process step(s) repaired defects that existed on the edge of the wafer before the intervening process step(s). Rather  
30           than comparing the defect data, however, the “before” and “after” recorded images

of the edge of the wafer may be directly compared to each other to locate any added or repaired defects.

For different wafers that have been inspected both before and after the same process step, the average performance of the process step, or the fabrication station 102-114 (Fig. 1), can be determined. If the process step needs to be adjusted, then both before-adjustment and after-adjustment inspection data can be generated. Upon comparing before-adjustment and after-adjustment inspection data together, the effect of the adjustment can be determined.

Three exemplary embodiments for the inspection station 124 are shown in Figs. 3, 4 and 5 with different wafer-handling techniques. Each of the inspection stations 124 has a housing 130. Each of the inspection stations 124 has similar image capturing devices 132 and 134, such as scanning electron microscopes, digital cameras, and the like, for capturing images of the edge of an exemplary wafer 136. Two image capturing devices 132 and 134 are shown, but in a particular embodiment, only one such image capturing device 132 or 134 is used. With more than one image capturing device 132 or 134, though, different sets of inspection data can be obtained almost simultaneously using different imaging techniques that may highlight different types of edge defects.

The wafer 136 sits on a chuck 138. The chuck 138 rotates the wafer 136 while the image capturing devices 132 and 134 scan the edge of the wafer 136 and capture images thereof. The image capturing devices 132 and 134 send image data through connection lines 140 and 142, respectively, to the database 126 (Fig. 2).

The inspection stations 124 include at least one robot arm 144 for moving each wafer 136 onto and off of the chuck 138. The Fig. 3 inspection station 124 further includes a conventional removable wafer cassette (or conventional wafer indexer) 146 which contains each wafer 136 that is to be inspected or has been inspected. The robot arm 144 moves each wafer 136 to be inspected from the wafer cassette 146 to the chuck 138 for inspection and back to the wafer cassette 146 after inspection.

The Fig. 4 inspection station 124 includes two removable wafer cassettes (or wafer indexers) 148 and 150. One of the wafer cassettes 148 contains each wafer 136 that is coming into the inspection station 124 to be inspected. The other wafer cassette 150 contains each wafer 136 that has been inspected and is leaving the inspection station 124. Thus, the robot arm 144 moves each incoming wafer 136 from the incoming wafer cassette 148 to the chuck 138 to be inspected and moves each inspected wafer 134 to the outgoing wafer cassette 150.

The Fig. 5 inspection station 124 includes a second robot arm 152. The first robot arm 144 moves each incoming wafer 136 from the incoming wafer cassette 148 to the chuck 138 to be inspected. The second robot arm 152 then moves each inspected wafer 136 from the chuck 138 to the outgoing wafer cassette 150.

Each configuration for the inspection station 124 (Figs. 3, 4 and 5) has a different speed or throughput capability and a tradeoff in space and cost requirements. Therefore, the selection of the configuration for the inspection station 124 depends on the cost/benefit for the desired wafer throughput.

Each wafer 136, as shown in Fig. 6, includes an orientation location point, such as a notch 154, etc. The inspection station 124 (Figs. 2-5) locates the notch 154 to orient the wafer 136 on the chuck 138 (Figs. 3-5) and then scans the edge 156 of the wafer 136 either for a full 360° from the notch 154 back to the notch 154 or for some smaller inspection area, such as a 90° or 180° section or some other range depending on whatever portion of the wafer 136 needs to be inspected. The image capturing device 132 and 134 then captures an image of the desired inspection area and transfers the image to the database 126 (Fig. 2).

A typical wafer 136, as shown in Fig. 7, has an edge, or bevel, 158 with a slight convex curvature. The top 160 and bottom 162 (at approximately 0° and 180°, respectively, of the curvature) of the edge 158 have a smaller radius of curvature than does the middle of the edge 158. The primary area of interest for edge inspection extends from a point on the top surface 164 of the wafer 136 slightly interior of the top 160 of the edge 158 to a point slightly exterior of the bottom 162 of the edge 158, or any portion thereof, as indicated by the arrow A.

The image capturing device 134, therefore, may have a field of view that incorporates the entire desired inspection area, or may be moved relative to the edge 158 along the arrow A to any angle at which a desired portion of the edge 158 is to be scanned.

5           The image capturing device 134 automatically scans the desired portion of the edge 158 of the wafer 136 and captures an image thereof. The image capturing device 134 preferably does this procedure according to a “recipe” that specifies various parameters that affect the image that will be captured. For instance, the recipe may include values for: the angle of the image capturing  
10       device 134 relative to the edge 158 of the wafer 136 along arrow A, the magnification of the image capturing device 134, the focus of the image capturing device 134 (given the curvature of the edge 158, every point in the area of interest may not be in focus at the same time), brightness of one or more illumination  
15       sources 166 that illuminate the edge 158 of the wafer 136 in the case that the image capturing device 134 is an optical device, portion of the edge 158 of the wafer 136 to be scanned (e.g. portion of arrow A), the rotational speed of the wafer 136 or the chuck 138 (Figs. 3-5), a gain setting on a photomultiplier sensor, contrast setting, the accelerating voltage for an electron beam and probe current in the event that the image capturing device 134 is a scanning electron microscope,  
20       the angular location of the desired sample area, and threshold values for determining a defect, among other possible parameters for the inspection recipe. The recipe, as well as the captured image, may be stored in the database 126 (Fig. 2) for each wafer 136 scanned, so the image analysis can take into account any of these parameters. Additionally, when comparing two different images, it may be  
25       preferable for the recipe to have been the same when capturing both images.

The results of defect analyses for two exemplary inspection procedures are shown graphically in Fig. 8. The first inspection procedure and analysis resulted in defect data 168 for a full 360° inspection area around the edge 158 (Figs. 6 and 7) of a wafer 136 (Figs. 3-7) and for a full primary area of interest, as described above

with reference to Fig. 7. The second inspection procedure and analysis resulted in defect data 170 for the same area.

The defect data 168 indicated that defects 172-180 were detected. The defect data 170, on the other hand, indicated that defects 172-178, 182 and 184 were detected. Since some of the detected defects 172-178 were the same for both defect data 168 and 170, it is apparent that, for this example, the two inspection procedures were performed on the same wafer 136 (Figs. 3-7) after different process steps. By effectively subtracting defect data 168 from defect data 170, the added defects 182 and 184 are exposed, as shown by added defect data 186. Thus, defects 182 and 184 were apparently added to the wafer 136 by the intervening process step(s). On the other hand, by effectively subtracting defect data 170 from defect data 168, the repaired defects 180 are exposed, as shown by repaired defect data 188. Thus, defects 180 were apparently repaired on the wafer 136 by the intervening process step(s).

It is apparent from the previous description that the present invention enables a robust wafer edge defect inspection system. The inspection has the advantage of being automated, so control is achieved simply by adjusting the inspection recipe. Additionally, a very detailed defect analysis can be performed to determine the effect of selected process steps on the condition of the edges of the wafers, so the wafers can be rerouted for repair or the process steps can be adjusted for improved performance. In this manner, the yield rate of the fabrication system 100 (Fig. 1) is improved. Furthermore, the inspection information is stored and readily accessible for any desired analysis at any time on any inspected wafer(s). Thus, the user can perform a detailed analysis on many parts of the fabrication system 100 after the fabrication system 100 has been in operation for any length of time in order to ensure proper functioning of the fabrication system 100 or debugging of potential problems that may arise upon initial assembly of the fabrication system 100 or at any other time.

Presently preferred embodiments of the present invention and many of its improvements have been described with a degree of particularity. This description

is of preferred examples of implementing the invention, and is not necessarily intended to limit the scope of the invention. The scope of the invention is defined by the following claims.